Errata Revision: *C

May 02, 2007

RAM9 QDR-I/DDR-I/QDR-II/DDR- II Errata

This document describes the $\overline{\text{DOFF}}$ issue for QDRII/DDRII and the Output Buffer and JTAG issues for QDRI/DDRI/QDRII/DDRII. Details include trigger conditions, possible workarounds and silicon revision applicability. This document should be used to compare to the respective datasheet for the devices to fully describe the device functionality.

Please contact your local Cypress Sales Representative for availability of the fixed devices and any other questions.

Devices Affected

Density & Revision	Part Numbers	Architecture
9Mb - Ram9(90 nm)	CY7C130*DV25	QDRI/DDRI
9Mb - Ram9(90 nm)	CY7C129*DV18	QDRII
18Mb - Ram9(90nm)	CY7C130*BV18 CY7C130*BV25 CY7C132*BV25	QDRI/DDRI
18Mb - Ram9(90nm)	CY7C131*BV18 CY7C132*BV18 CY7C139*BV18 CY7C191*BV18	QDRII/DDRII
36Mb - Ram9(90nm)	CY7C141*AV18 CY7C142*AV18	QDRII/DDRII
72Mb -Ram9(90nm)	CY7C151*V18 CY7C152*V18	QDRII/DDRII

Table 1. List of Affected devices

Product Status

All of the above densities and revisions are available in sample as well as production quantities.

QDR/DDR $\overline{\text{DOFF}}$ Pin, Output Buffer and JTAG Issues Errata Summary

The following table defines the issues and the fix status for the different devices which are affected.

Item	Issue	Device	Fix Status
1.	$\overline{\text{DOFF}}$ pin is used for enabling/disabling the DLL circuitry within the SRAM. To enable the DLL circuitry, $\overline{\text{DOFF}}$ pin must be externally tied HIGH. The QDR-II/DDR-II devices have an internal pull down resistor of ~5KΩ. The value of the external pull-up resistor should be 500Ω or less in order to ensure DLL is enabled.	9Mb - “D” Rev - Ram9 18Mb - “B” Rev - Ram9 36Mb - “A” Rev - Ram9 72Mb - Ram9 QDR-II/DDR-II Devices	The fix involved removing the internal pull-down resistor on the $\overline{\text{DOFF}}$ pin. The fix has been implemented on the new revision and is now available.

Item	Issue	Device	Fix Status
2.	O/P Buffer enters a locked up undefined state after controls or clocks are left floating. No proper read/write access can be done on the device until a dummy read is performed.	9Mb - “D” Rev - Ram9 18Mb - “B” Rev - Ram9 36Mb - “A” Rev - Ram9 72Mb - Ram9 QDR-I/DDR-I/ QDR-II/DDR-II Devices	The fix has been implemented on the new revision and is now available.
3.	The EXTEST function in the JTAG test fails when input K clock is floating in the JTAG mode.	9Mb - “D” Rev - Ram9 18Mb - “B” Rev - Ram9 36Mb - “A” Rev - Ram9 72Mb - Ram9 QDR-I/DDR-I/ QDR-II/DDR-II Devices	The fix involved bypassing the ZQ circuitry in JTAG mode. This was done by overriding the ZQ circuitry by the JTAG signal. The fix has been implemented on the new revision and is now available.

Table 2. Issue Definition and fix status for different devices

1. $\overline{\text{DOFF}}$ Pin Issue

- ISSUE DEFINITION

  This issue involves the DLL not turning ON properly if a large resistor is used (eg:-10KΩ) as an external pullup resistor to enable the DLL. If a 10KΩ or higher pullup resistor is used externally, the voltage on $\overline{\text{DOFF}}$ is not high enough to enable the DLL.
- PARAMETERS AFFECTED

  The functionality of the device will be affected because of the DLL is not turning ON properly. When the DLL is enabled, all AC and DC parameters on the datasheet are met.
- TRIGGER CONDITION(S)

  Having a 10KΩ or higher external pullup resistor for disabling the $\overline{\text{DOFF}}$ pin.
- SCOPE OF IMPACT

  This issue will alter the normal functionality of the QDRII/DDRII devices when the DLL is disabled.
- EXPLANATION OF ISSUE

  Figure 1 shows the $\overline{\text{DOFF}}$ pin circuit with an internal 5KΩ internal resistor. The fix planned is to disable the internal 5KΩ leaker.

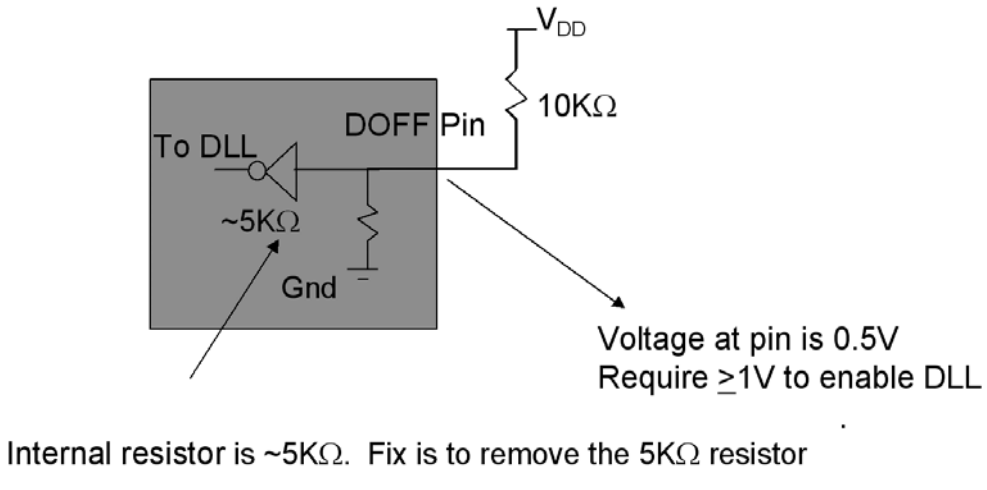

Figure 1. $\overline{\text{DOFF}}$ pin with the 5KΩ internal resistor

- WORKAROUND

The workaround is to have a low value of external pullup resistor for the $\overline{\text{DOFF}}$ pin (recommended value is ≤500Ω). When DOFF pins from multiple QDR devices are connected through the same pull-up resistors on the board, it is recommended that this $\overline{\text{DOFF}}$ pin be directly connected to Vdd due to the lower effective resistance since the "leakers" are in parallel.

Figure 2 shows the proposed workaround and the fix planned.

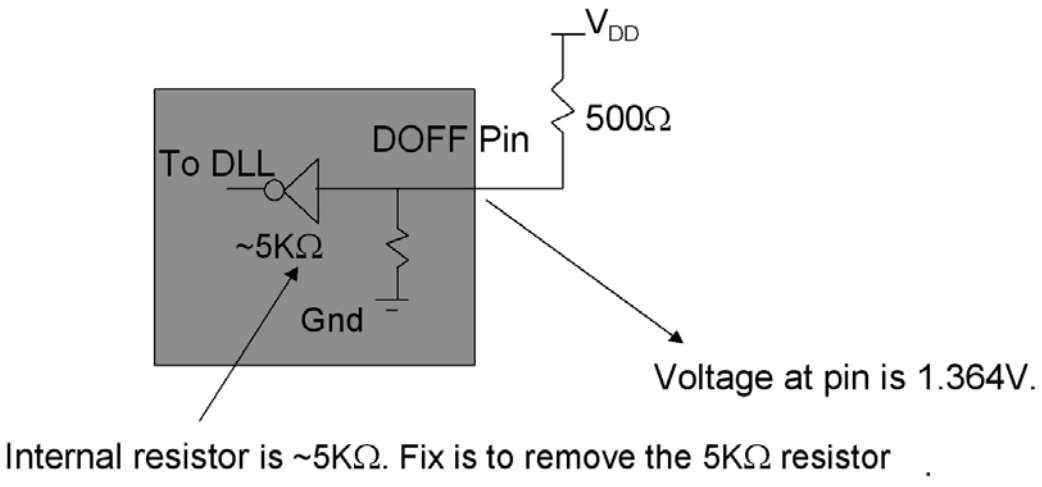

Figure 2. Proposed workaround with the 500Ω external pullup

- FIX STATUS

  Fix involved removing the internal pull-down resistor on the $\overline{\text{DOFF}}$ pin. The fix has been implemented on the new revision and is now available. The new revision is an increment of the existing revision. The following table lists the devices affected, current revision and the new revision after the fix.

Current Revision	New Revision after the Fix
CY7C129*DV18	CY7C129*EV18
CY7C131*BV18	CY7C131*CV18
CY7C132*BV18	CY7C132*CV18
CY7C139*BV18	CY7C139*CV18
CY7C191*BV18	CY7C191*CV18
CY7C141*AV18	CY7C141*BV18
CY7C142*AV18	CY7C142*BV18
CY7C151*V18	CY7C151*AV18
CY7C152*V18	CY7C152*AV18

Table 3. List of Affected Devices and the new revison

2.Output Buffer Issue

- ISSUE DEFINITION

  This issue involves the output buffer entering an unidentified state when the input signals (only Control signals or Clocks) are floating during reset or initialization of the memory controller after power up.
- PARAMETERS AFFECTED

  No timing parameters are affected. The device may drive the outputs even though the read operation is not enabled. A dummy read is performed to clear this condition.
- TRIGGER CONDITION(S)

  Input signals(namely RPS# for QDR-I/QDRII , WE# and LD# for DDR-I/DDRII) or Clocks (K/K# and/or C/C#) are floating during reset or initialization of the memory controller after power up.
- SCOPE OF IMPACT

  This issue will jeopardize any number of writes or reads which take place after the controls or clock are left floating. This can occur anywhere in the SRAM access (all the way from power up of the memory device to transitions taking place for read/write accesses to the memory device) if the above trigger conditions are met.
- EXPLANATION OF ISSUE

  Figure 3 shows the output register Reset circuit with an SR Latch circled. This latch has two inputs with one of them coming from some logic affected by the clock and RPS#(QDR) or WE# and LD#(DDR).The issue happens when clocks are glitching/toggling with controls floating. This will cause the SR latch to be taken into an unidentified state. The SR Latch will need to be reset by a dummy read operation if this happens.

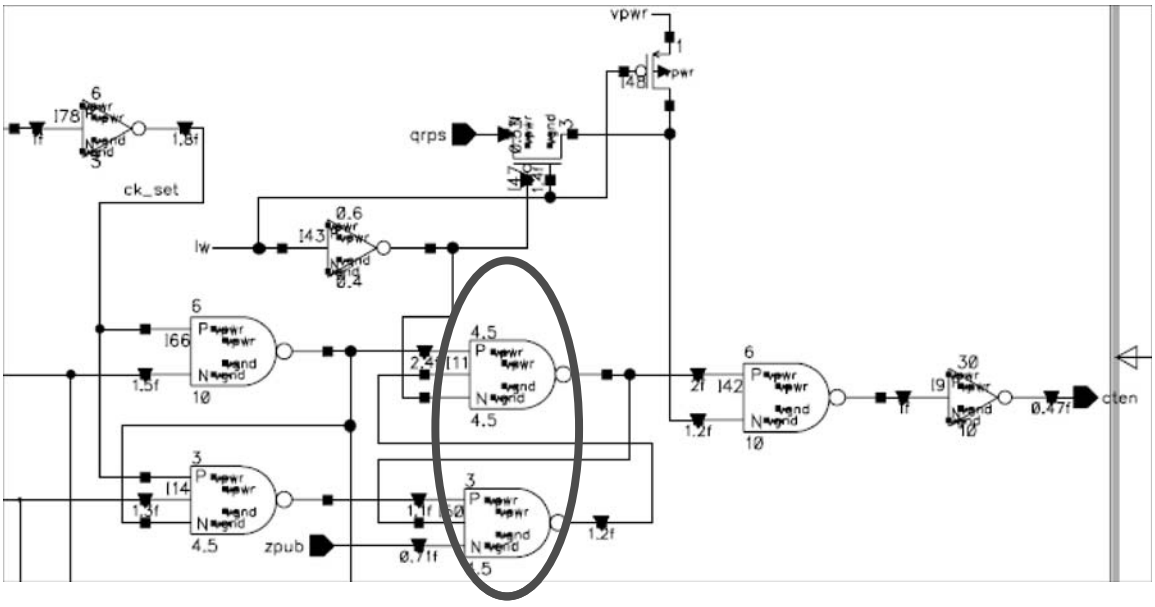

Figure 3. Output Register Reset Circuit

- WORKAROUND

  This is viable only if the customer has the trigger conditions met during reset or initialization of the memory controller after power up. In order for the workaround to perform properly, Cypress recommends the insertion of a minimum of 16 “dummy” READ operations to every SRAM device on the board prior to writing any meaningful data into the SRAM. After this one “dummy” READ operation, the device will perform properly. “Dummy” READ is defined as a read operation to the device that is not meant to retrieve required data. The “dummy” READ can be to any address location in the SRAM. Refer to *Figure 4* for the dummy read implementation.

In systems where multiple SRAMs with multiple RPS# lines are used, a dummy read operation will have to be performed on every SRAM on the board. Below is an example sequence of events that can be performed before valid access can be performed on the SRAM.

1) Initialize the Memory Controller

2) Assert RPS# Low for each of the memory devices

Note:

For all devices with x9 bus configuration, the following sequence needs to be performed:

1) For the 72M / 36M / 18M x9 devices drive address pin A2 / A10 / A3 low respectively and perform dummy read.

2) For the 72M / 36M / 18M x9 devices drive address pin A2 / A10 / A3 high respectively and perform dummy read.

If the customer has the trigger conditions met during normal access to the memory then there is no workaround at this point.

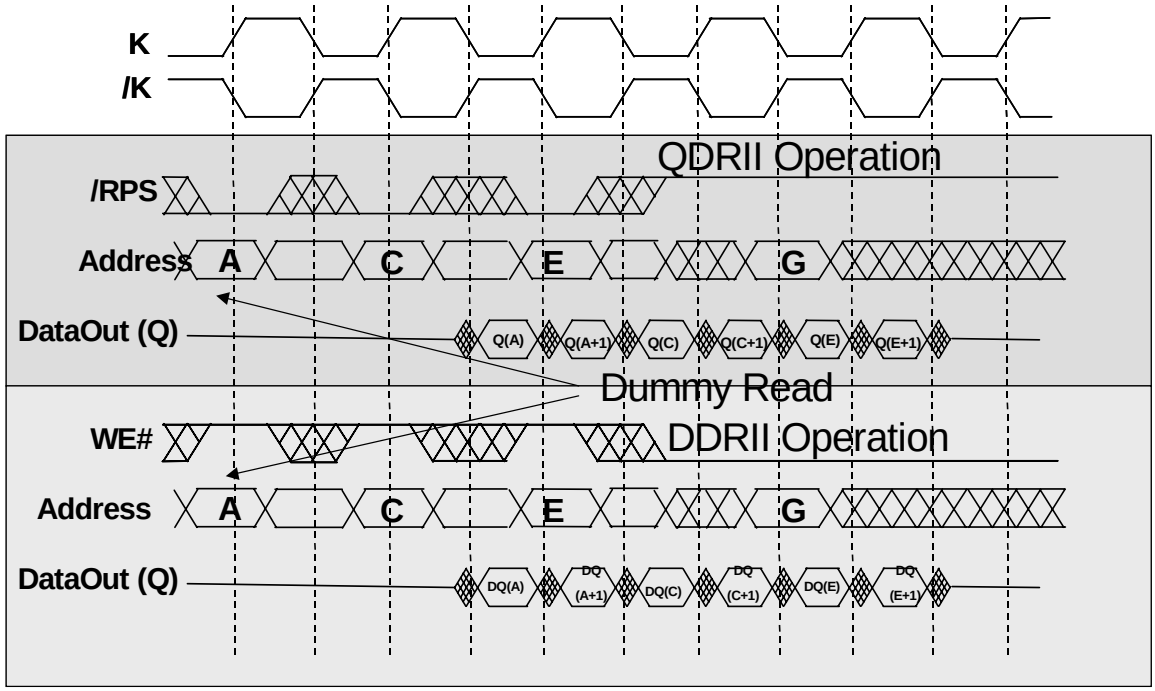

Figure 4. Dummy Read Implementation

- FIX STATUS

  The fix has been implemented on the new revision and is now available. The new revision is an increment of the existing revision. Please refer to Table 4 for the list of devices affected, current revision and the new revision after the fix.

3. JTAG Mode Issue

- ISSUE DEFINITION

  If the input clock (K Clock) is left floating when the device is in JTAG mode, spurious high frequency noise on this input can be interpreted by the device as valid clocks. This could cause the impedance matching circuitry (ZQ) on the QDR/DDR devices to periodically load itself with incorrect values. These incorrect values in the ZQ register could force the outputs into a High-Impedance state. The ZQ circuitry requires at least 1000 valid K clock cycles to drive the outputs from high impedance to low impedance levels.

- PARAMETERS AFFECTED

This issue only affects the EXTEST command when the device is in the JTAG mode. The normal functionality of the device will not be affected.

- TRIGGER CONDITION(S)

  EXTEST command executed immediately after power-up without providing any K clock cycles.
- SCOPE OF IMPACT

  This issue only impacts the EXTEST command when device is tested in the JTAG mode. Normal functionality of the device is not affected.
- EXPLANATION OF ISSUE

  Impedance matching circuitry (ZQ) is present on the QDR/DDR devices to set the desired impedance on the outputs. This ZQ circuitry is updated every 1000 clock cycles of K clock to ensure that the impedance of the O/P is set to valid state. However, when the device is operated in the JTAG mode immediately after power-up, high frequency noise on the input K clock can be treated by the ZQ circuitry as valid clocks thereby setting the outputs in to a high-impedance mode. If a minimum of 1000 valid K clocks are applied before performing the JTAG test, this should clear the ZQ circuitry and ensure that the outputs are driven to valid impedance levels.
- WORKAROUND

  Elimination of the issue: After power-up, before any valid operations are performed on the device, insert a minimum of 1000 valid clocks on K input.
- FIX STATUS

  The fix involved bypassing the ZQ circuitry in JTAG mode. This was done by overriding the ZQ circuitry by the JTAG signal. The fix has been implemented on the new revision and is now available. The new revision is an increment of the existing revision. Please refer to Table 4 for the list of devices affected, current revision and the new revision after the fix..

Current Revision	New Revision after the Fix
CY7C129*DV18	CY7C129*EV18
CY7C130*DV25	CY7C130*EV25
CY7C130*BV18	CY7C130*CV18
CY7C130*BV25	CY7C130*CV25
CY7C132*BV25	CY7C132*CV25
CY7C131*BV18	CY7C131*CV18
CY7C132*BV18	CY7C132*CV18
CY7C139*BV18	CY7C139*CV18
CY7C191*BV18	CY7C191*CV18
CY7C141*AV18	CY7C141*BV18
CY7C142*AV18	CY7C142*BV18
CY7C151*V18	CY7C151*AV18
CY7C152*V18	CY7C152*AV18

Table 4. List of Affected devices and the new revision

References

All 90nm QDRI/DDRI/QDRII/DDRII datasheets:-

Spec#	Part#	Density	Architecture
38-05628	CY7C1304DV25	9-MBIT	QDR(TM) SRAM 4-WORD BURST
38-05632	CY7C1308DV25	9-MBIT	DDR-I SRAM 4-WORD BURST
001-00350	CY7C1292DV18/1294DV18	9-MBIT	QDR- II(TM) SRAM 2-WORD BURST
38-05621	CY7C1316BV18/1916BV18/1318BV18/1320BV18	18-MBIT	DDR-II SRAM 2-WORD BURST
38-05622	CY7C1317BV18/1917BV18/1319BV18/1321BV18	18-MBIT	DDR-II SRAM 4-WORD BURST
38-05623	CY7C1392BV18/1393BV18/1394BV18	18-MBIT	DDR-II SIO SRAM 2-WORD BURST
38-05631	CY7C1323BV25	18-MBIT	DDR-I SRAM 4-WORD BURST
38-05630	CY7C1305BV25/1307BV25	18-MBIT	QDR(TM) SRAM 4-WORD BURST
38-05627	CY7C1303BV25/1306BV25	18-MBIT	QDR(TM) SRAM 2-WORD BURST
38-05629	CY7C1305BV18/1307BV18	18-MBIT	QDR(TM) SRAM 4-WORD BURST
38-05626	CY7C1303BV18/1306BV18	18-MBIT	QDR(TM) SRAM 2-WORD BURST
38-05619	CY7C1310BV18/1910BV18/1312BV18/1314BV18	18-MBIT	QDR - II (TM) SRAM 2-WORD BURST
38-05620	CY7C1311BV18/1911BV18/1313BV18/1315BV18	18-MBIT	QDR - II SRAM 4-WORD BURST
38-05615	CY7C1410AV18/1425AV18/1412AV18/ 1414AV18	36-MBIT	QDR-II(TM) SRAM 2-WORD BURST
38-05614	CY7C1411AV18/1426AV18/1413AV18/ 1415AV18	36-MBIT	QDR(TM)-II SRAM 4-WORD BURST
38-05616	CY7C1416AV18/1427AV18/1418AV18/1420AV18	36-MBIT	DDR-II SRAM 2-WORD BURST
38-05618	CY7C1417AV18/1428AV18/1419AV18/1421AV18	36-MBIT	DDR-II SRAM 4-WORD BURST
38-05617	CY7C1422AV18/1429AV18/1423AV18/1424AV18	36-MBIT	DDR-II SIO SRAM 2-WORD BURST
38-05489	CY7C1510V18/1525V18/1512V18/1514V18	72-MBIT	QDR-II SRAM 2-WORD BURST
38-05363	CY7C1511V18/1526V18/1513V18/1515V18	72-MBIT	QDR(TM)-II SRAM 4-WORD BURST
38-05563	CY7C1516V18/1527V18/1518V18/1520V18	72-MBIT	DDR-II SRAM 2-WORD BURST
38-05565	CY7C1517V18/1528V18/1519V18/1521V18	72-MBIT	DDR-II SRAM 4-WORD BURST
38-05564	CY7C1522V18/1529V18/1523V18/1524V18	72-MBIT	DDR-II SIO SRAM 2-WORD BURST

Table 5. List of Datasheet spec# for the Affected devices

Document History Page

Document Title: RAM9 QDR-I/DDR-I/QDR-II/DDR- II Errata Document #: 001-06217 Rev. *C				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	419849	See ECN	REF	New errata for Ram9 QDR2/DDR2 SRAMs.
*A	493936	See ECN	QKS	Added Output buffer and JTAG mode issues, Item#2 and #3 Added 9Mb QDR-II Burst of 2 and QDR-1/DDR-I part numbers.
*B	733176	See ECN	NJY	Added missing part numbers in the title for Spec#'s 38-05615,38-05614, 38-05363,38-05563 on Table 5 on page 7.
*C	1030020	See ECN	TBE	Updated the fix status of the three issues, and modified the description for the Output Buffer workaround for x9 devices on page 5.